THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte KARL M. GUTTAG, KEITH BALMER,
ROBERT J. GOVE, CHRISTOPHER J. READ, JEREMIAH E. GOLSTON,
SYDNEY W. POLAND, NICHOLAS ING-SIMMONS and PHILLIP MOYSE

_____

Appeal No. 96-3494
Application 08/160,299[1]

_____

ON BRIEF

_____

Before HAIRSTON, KRASS and JERRY SMITH, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

_____

[1] Application for patent filed November 30, 1993.

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-34, which constitute all the claims in the application. Appellants have indicated that the appeal is withdrawn with respect to claim 34 [brief, page 2]. Accordingly, this appeal now involves only claims 1-33.

The claimed invention pertains to a data processing apparatus having an arithmetic logic unit (ALU) with three separate multibit digital inputs. The ALU performs mixed arithmetic and Boolean operations on the three inputs. A barrel rotator is connected to one of the three inputs for rotating the digital signal received at that input. A function control input to the ALU determines which operations will be performed on the three multibit digital inputs received by the ALU.

Representative claim 1 is reproduced as follows:

1. A data processing apparatus comprising:

an arithmetic logic unit having first, second and third data inputs for multibit digital signals representing corresponding first, second and third input signals, and a function control input signal for receiving a function signal, said arithmetic logic unit generating at an output a multibit digital signal representing a mixed arithmetic and Boolean combination of said first, second and third inputs

corresponding to said function signal, said mixed arithmetic and Boolean combination including at least an arithmetic combination of only said first and second inputs and an arithmetic combination of only said first and third inputs;

a first data source supplying a first multibit digital signal to said first data input of said arithmetic logic unit;

a second data source supplying a second multibit digital signal;

a barrel rotator having a data input connected to said second data source, a rotate control input receiving a rotate control signal, and a data output connected to said second data input of the arithmetic logic unit, said barrel rotator left rotating said second multibit digital signal an amount corresponding to said rotate control signal and supplying said left rotated second multibit digital signal to said second data input of said arithmetic logic unit; and

a third data source supplying a third multibit digital signal to said third data input of said arithmetic logic unit.

The examiner relies on the following references:

Chu et al. (Chu)	4,785,393	Nov. 15, 1988
Pfeiffer et al. (Pfeiffer)	5,146,592	Sep. 08, 1992
Vassiliadis et al. (Vassiliadis)	5,299,319	Mar. 29, 1994 (filed Mar. 29, 1991)

Claims 1-33 stand rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the invention. Claims 1-33 also stand provisionally rejected under 35 U.S.C. § 101 as claiming the

same invention as claims 1-9, 40-48 and 79-93 of copending application Serial No. 08/160,111. Claims 1, 7-10, 16-18 and 31-33 stand rejected under 35 U.S.C. § 103 as unpatentable over the teachings of Chu and Vassiliadis. Finally, claims 19-30 stand rejected under 35 U.S.C. § 103 as unpatentable over the teachings of Chu, Vassiliadis and Pfeiffer.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness and double patenting relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that claims 1-33 comply with the requirements of the second paragraph of 35 U.S.C. § 112. We are also of the view that the provisional double patenting rejection of claims 1-33 should be reversed. Finally, we are of the view that the collective evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1, 7-10 and 16-33. Accordingly, we affirm-in-part.

We consider first the rejection of claims 1-33 under the second paragraph of 35 U.S.C. § 112. The examiner asserts that the second "and" in claim 1, line 10 and in claim 10, line 16 is confusing in light of appellants' disclosure. The examiner also asserts that the scope of the phrase "a predetermined one of said plurality of data registers" in claims 2 and 11 is vague and indefinite [answer, page 3]. Appellants argue that the examiner's position is erroneous and explain why the claims satisfy the requirements of 35 U.S.C. § 112. We agree with appellants for the reasons indicated by them. The examiner is misreading the claims in order to support the rejection. The scope of the claims would be clear

to the artisan as argued by appellants. Therefore, we do not sustain this rejection of claims 1-33.

We now consider the provisional rejection of claims 1-33 under 35 U.S.C. § 101 as claiming the same invention as claims 1-9, 40-48 and 79-93 of copending application Serial No. 08/160,111.

Appellants refer to this rejection as a "provisional obviousness type double patenting rejection," and indicate that the rejection should be held in abeyance until all other issues have been resolved in accordance with the procedure of MPEP § 804 [brief, page 4]. The section of the MPEP referred to by appellants merely provides guidance to the examiner as to what to do when an application is otherwise ready for allowance except for the double patenting rejection. The MPEP does not relieve an applicant of the burden of arguing the merits of the rejection. In fact, section 804 specifically states that the merits of a provisional double patenting rejection can be addressed by the examiner and applicant without waiting for a patent to issue [page 800-15, section B]. Thus, the merits of the double patenting rejection can be

considered even though there are other rejections pending against the claims.

At the outset we note that the examiner's rejection is not based on obvious double patenting. Rather, the rejection indicates that it is based on the same invention type double patenting of 35 U.S.C. § 101. A rejection on this basis requires that the two inventions be exactly the same and not simply patentably indistinct. The claims of copending application Serial No. 08/160,111 are different from the claims of this application in that each corresponding claim of the copending application recites a mask generator in addition to the elements recited in the claims of this application. Thus, the claims of this application and the copending application are not of exactly the same scope because the claims of the copending application recite an additional element. The only legally applicable double patenting rejection on this record would be a rejection of the obviousness-type. Such a rejection is not before us, however, and we do not consider it. We are constrained on this record to reverse the examiner's provisional rejection of claims 1-33 on the ground of double patenting under 35 U.S.C. § 101.

We now consider the rejection of claims 1, 7-10 and 16-33 under 35 U.S.C. § 103. As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We now consider the rejection of claim 1 as unpatentable over Chu and Vassiliadis. Claims 9, 10, 18 and 31-33 are grouped with claim 1 and will stand or fall with claim 1 [brief, page 3]. The examiner has pointed out that Chu teaches an ALU which performs mixed arithmetic and logical operations on three inputs received at the ALU. The examiner indicates that Chu does not teach the claimed operations

performed only on the first and second inputs and on the first and third inputs [answer, pages 4-5]. The examiner cites Vassiliadis to teach an ALU which performs mixed arithmetic and logical operations on any two inputs of a three input ALU. The examiner also explains why it would have been obvious to the artisan to replace the Chu ALU with the Vassiliadis ALU. In our view, the examiner has at least presented a prima facie case of the obviousness of claim 1. Therefore, we consider appellants' arguments and the relative persuasiveness of the arguments.

Appellants' first argument is that Chu does not teach the claimed ALU for performing the operations A±B and A±C as recited in claim 1. The examiner has acknowledged this deficiency in Chu which is why the reference was combined with Vassiliadis. Appellants argue that Vassiliadis also does not provide this teaching because Vassiliadis teaches that two operand ALU functions are achieved by forcing one input to zero [brief, page 7]. According to appellants, claim 1 recites that the ALU combinations are achieved by control of the function of the ALU and not by forcing one input to zero.

Based on this argument, appellants assert that claim 1 is not suggested by the collective teachings of Chu and Vassiliadis.

In our view, appellants' interpretation of claim 1 is not commensurate with the language of claim 1. Claim 1 does not require that the two operand functions be implemented in any specific manner. Claim 1 only recites that the ALU receive a control function input and that the ALU perform the operations A±B and A±C. The ALUs of Chu and Vassiliadis clearly receive an input function control signal, and Vassiliadis clearly performs the noted operations as pointed out by the examiner. Appellants are attempting to import their disclosed preferred embodiment into the claim which is not appropriate. Claims are given their broadest reasonable interpretation during prosecution before the Patent and Trademark Office.

Since we have determined that the examiner has presented a prima facie case for the obviousness of claim 1, and since appellants have not presented a compelling reason to find error in the examiner's case, we sustain the rejection of claim 1 and of claims 9, 10, 18 and 31-33 which are grouped therewith.

We now consider the rejection of claims 7 and 16 which are grouped together. Claim 7 depends from claim 1 and recites that a plurality of data registers receives an input from the output of the ALU and an input from the output of the barrel rotator. The examiner has provided a reasonable analysis as to why the presence of registers, as broadly recited in claim 7, would have been obvious to the artisan in view of the applied prior art. Appellants argue that Chu does not show such a register at the output of the barrel rotator, but this argument fails to address the obviousness of broadly providing such a register. Appellants also argue that "claims 7 and 16 require storage of both the output of the arithmetic logic unit and the output of the shifter [sic, barrel rotator] during the same operation. Neither Chu et al nor Vassiliadis et al show the claimed simultaneous storage of these two outputs in any mode" [brief, page 7]. We agree with the examiner that this argument of appellants is not commensurate in scope with the claimed invention. We find nothing in claim 7 which requires the simultaneous storage as argued by appellants. Since appellants' arguments are not persuasive of

error by the examiner, we sustain the rejection of claims 7 and 16.

With respect to claims 8 and 17 which are grouped together, the examiner asserts that Chu teaches a one's constant source to supply a barrel rotator [answer, page 5]. Appellants argue that insertion of 1's into the shifter of Chu does not make obvious the specific digital signal whose value is "0001" as recited in claim 8 [brief, page 8]. The examiner responds that Chu can provide a single bit of value "1" to the shifter which would meet the recitation of claim 8 [answer, page 8]. Appellants reply that the prior art does not recognize the problem and does not make the claimed invention obvious [reply brief, pages 4-5].

When the scope of claim 8 is considered, we agree with the examiner that the broad recitation of applying a data input of value "0001" would have been obvious to the artisan in view of Chu's teaching of inserting 1's into the shifter 118. We are of the view that the artisan would have recognized the obviousness of making any number of the least significant bits "1" based upon the amount of shift or

rotation desired. Therefore, we sustain the rejection of claims 8 and 17.

We now consider the rejection of claims 19-30 as unpatentable over the teachings of Chu, Vassiliadis and Pfeiffer. Although appellants nominally indicated that these claims were grouped with claim 10, this rejection includes the additionally applied Pfeiffer reference so that the nominal grouping is technically not applicable. The only argument offered by appellants for the patentability of these claims is that they incorporate the limitations of claim 10 by dependence. Since we have previously determined that the rejection of claim 10 would be sustained, and since appellants have offered no compelling reason for the patentability of claims 19-30, we also sustain the Section 103 rejection of these claims.

In summary, the provisional double patenting rejection of claims 1-33 under 35 U.S.C. § 101 is not sustained. The rejection of claims 1-33 under the second paragraph of 35 U.S.C. § 112 is also not sustained. The rejection of claims 1, 7-10 and 16-33 under 35 U.S.C. § 103 is sustained.

Accordingly, the decision of the examiner rejecting claims 1-33 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)
ERROL A. KRASS Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES

)
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